CLAIMS

1. A signal flow driven circuit analysis technique by tracing circuit signal flow so that, analyzing a circuit, and partitioning a circuit based on functionality and criticality, and generating multitude circuit layout constraints are done by software program automatically.

2. A signal flow driven circuit physical synthesis technique by tracing circuit signal flow so that, placing and routing circuit cell physical layout based on giving critical signal path with high priority are done by software program automatically.

3. An analytical parasitic constraint generation technique for layout constraint generation using open circuit time constant technique on multitude critical nodes.

4. A analytical parasitic constraint generation technique of claim 3 comprising:
   (a) Providing a memory that is able to store a circuit netlist employing input and output pins, any other terminal pins, power and ground terminals, active device elements, and passive device elements; and
   (b) Storing said circuit netlist in said memories; and
   (c) Providing a memory that is able to store a series of design specifications in said memory; and
   (d) Storing said series of design specifications in said memory; and
   (e) Calculating equivalent resistive impedance at each circuit node of said circuit netlist by performing DC operating point simulation using a numerical simulator such as SPICE; and
   (f) Calculating equivalent resistive impedance at each circuit node of said circuit netlist by performing transient simulation using a numerical simulator such as SPICE; and
   (g) Utilizing the analytical parasitic constraint generation technique of claim 3 wherein said the open circuit time constant technique to assessing a time constant of each circuit node; and

(h) Providing a memory that is able to store a bandwidth estimation module in said memory; and

(i) Storing said bandwidth estimation module in said memory; and

(j) Utilizing said bandwidth estimation module to estimates a circuit bandwidth based on said time constant at each circuit node and said circuit bandwidth will be compared with said series of design specification; and

(k) Providing a memory that is able to store a parasitic loading constraints generator in said memory; and

(l) Storing said parasitic loading constraints generator in said memory; and

(m) Utilizing said parasitic loading constraints generator to calculates a tolerable excessive parasitic loading at each circuit node for circuit physical synthesis at initial topology exploration stage.

5. A mean of circuit physical synthesis utilizing:
   (a) The analytical parasitic constraint generation technique of claim 3; and
   (b) The signal flow driven circuit physical synthesis technique of claim 2; and
   (c) The signal flow driven circuit analysis technique of claim 1.

6. A mean of selecting optimal circuit topology utilizing the analytical parasitic constraint generation technique of claim 3 wherein said parasitic loading constraints.

7. A mean of selecting optimal parasitic capacitance utilizing the analytical parasitic constraint generation technique of claim 3 wherein said parasitic loading constraints for optimized tuning frequency response of a RF circuit.

8. A mean of selecting optimal parasitic inductance utilizing the analytical parasitic constraint generation technique of claim 3 wherein said parasitic loading constraints for optimized tuning frequency response of a RF circuit.

9. A mean of stability analysis utilizing the analytical parasitic constraint generation technique of claim 3 wherein said parasitic loading constraints to generate an optimal range of the parasitic loading values.

10. A mean of optimizing circuit performance utilizing the analytical parasitic constraint generation technique of claim 3 quickly and analytically by running through what-if scenarios of placement options.

11. A mean of selecting optimal routing solution utilizing the analytical parasitic constraint generation technique of claim 3 quickly and analytically by running through what-if scenarios.

12. A mean of identifying a dominant pole[s] utilizing the analytical parasitic constraint generation technique of claim 3 for assessing the speed of an unknown circuit.